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Detection Of Arrhythmia By Ecg Signal And Its Implementation

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Abstract: ***Electrocardiogram (ECG) is an important biomedical signal which shows the electrical activity of heart. ECG waveform provides the valuable information for detection of abnormal heart diseases. A VLSI based modified arithmetic discrete wavelet transform for arrhythmia detection and its FPGA implementation. Time and frequency variations of QRS complex in ECG signal are identified. Then comparing this with normal ECG and identifying whether the patient is having arrhythmia or not. The modified discrete wavelet transform is used for compressing the ECG signal so it only consumes area of 6% and faster than the other approaches.***

Keywords: ECG, Modified DA DWT, LUTs, QRS complex

I. INTRODUCTION

Arrhythmia is a heart disorder which is a irregularity in heartbeat, the heart may beat either too fast or slow. Arrhythmia can take place in healthy heart and of minimal consequence but they may also indicate a serious problem that may lead to stroke or sudden cardiac death. Electrocardiogram is used by the cardiologist to analyze the ECG waveforms in diagnosis of various diseases and monitoring the conditions associated with heart. It is obtained by placing electrodes on the skin of the patient. It provides information about the disturbance in the heart rhythm. Any disorder of heart rate change in the morphological pattern is a reading of cardiac arrhythmia, after measure could be detected by analysis of ECG waveform. Normally continuous evaluation of the ECG is required to detect arrhythmia and is difficult because of the lengthy ECG record. Information regarding this disorder can be obtained from the variations in the length and the width of the QRS complex.

First of all necessary to remove the noise in the ECG signal that is caused due to the disturbances caused during the ECG measurement using the electrodes. The initial process involved in processing the ECG signal is to remove such variations using appropriate filtering methods. The timing and frequency information of this signal is extracted and the compared with the timing and frequency information of the normal patient by DWT so as to detect the presence of arrhythmia.

Morphological filtering is used to remove the unnecessary noise present in the ECG signal. Morphological operation transforms complex shapes into meaningful representations. The operation that involved in this are erosion, dilation, opening and closing. The morphological signal condition is performed and the results are verified in MATLAB.
After the removal of noise by morphological filtering, then a

modified distributive arithmetic DWT is used for the feature extraction of the ECG signal. The simulations were done on modelsim and finally the bit stream generated was downloaded to spartens 3 FPGA.
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I. MODIFIED DA DWT ARCHITECTURE

This is one of the technique that used for feature extraction from the images. By exploiting the symmetric property of the wavelet coefficients the number of LUTs and shift registers are reduced.

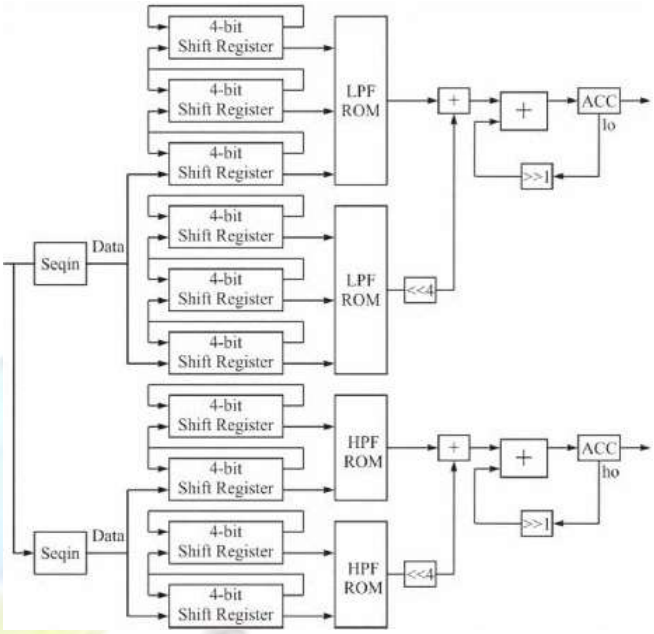

Figure 1 Modified Da Dwt

One of the most popular schemes suitable on FPGA is DA-DWT, it consumes fewer resources and have high throughput. A control logic designed loads the input data into the FPGA from external memory. LUT contents are read out based on the input samples as address to LUT. After 8 clock cycles of initial latency, DWT outputs are computed every clock cycle. In parallel implementation, the input data is divided into even samples and the odd samples based on their position. This scheme reduces the memory size to half due to the symmetric property of the filter coefficients. This increases the through put as the input samples are simultaneously used to read the data from two LUTs and hence speed is increased. In order to increase the speed and reduce the area modified DA-DWT is used. It consists of four LUTs each of them is accessed by even and odd samples of input matrix. Odd and even input samples are divided into 4bits of LSB and USB. In 1st stage input samples are split into even and odd then the data is sequentially loaded into serial in serial out shift registers, top four shift register stores MSB bits and the bottom four stores LSB bits. 40 clock cycles are needed to load shift register contents. At the end of the 40th clock cycle control logic configures the shift register as serial in parallel out forming address for LUTs.

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The output stage consists of adder's accumulators and right shift registers that are used to accumulate the LUTs contents and thus produces the output. This architecture has a latency of 44 clock cycle in computing first filter coefficients, and has a throughput of 4 clock cycles. This architecture is faster than other as the latency is reduced by half clock cycle and throughput is increased by a factor 2.

II. SIMULATION RESULTS

Modelsim simulation result is used fpr the proposed design is presented in figure 2 for the comparison of normal ECG with input ECG. Figure 3 represents the peak detection of ECG signal in MATLAB

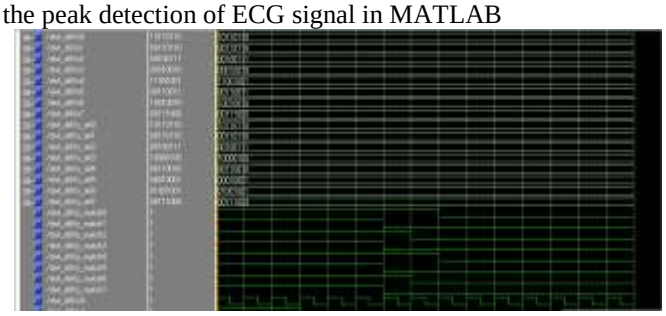

Figure 2 Arrhythmia Detection

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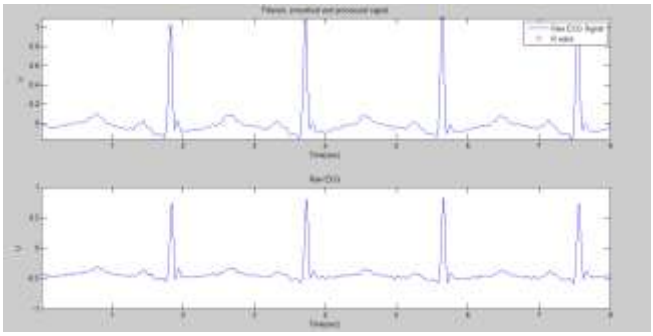

Figure 3 Peak Detection

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	551	5472	10%
Number of Slice Flip Flops	528	10944	4%
Number of 4 input LUTs	826	10944	7%
Number of bonded IOBs	138	240	57%
Number of DCMs	1	12	8%
Number of DSP48s	12	12	100%

figure 4 device utilization

III. CONCLUSION

Arrhythmia detection system and its implementation on FPGA using modified distributive arithmetic discrete wavelet transform. Using this transform amount of noise present in the ECG signal is removed and important features are extracted. This system is efficient in terms of reducing the calculation time and area.

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